

<b>Form PTO-1449</b>  <b>INFORMATION DISCLOSURE STATEMENT</b>				<b>Complete if Known</b>	
				Application No.:	not yet assigned
				Filing Date:	
				First Named Inventor:	Richard FOSS
				Group Art Unit:	
Examiner Name:					
Sheet	1	of	2	Attorney Docket No.:	PAT 819-2

### U.S. PATENT DOCUMENTS

Examiner Initials	Cite No.	Document No.	Date of Publication mm-dd-yyyy	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
GL		4,942,575	07-17-1990	Earnshaw et al.	
		4,901,320	02-13-1990	Sawada et al.	
		6,185,718	02-06-2001	Dell et al.	
		6,233,717	05-15-2001	Choi	
		6,353,910	03-05-2002	Carnevale et al.	
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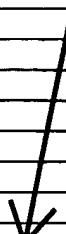
### OTHER DOCUMENTS

GL		P. Mazumder, "An On-Chip ECC Circuit for Correcting Soft Errors in DRAM's with Trench Capacitors", IEEE Journal of Solid-State Circuits, Vol. 27, No. 11, November 1992, pages 1623-1633.
		ISSCC 83, Friday, February 25, 1983, Imperial Ballroom A, 11:45am., Session XVI: 256K DRAMs, "FAM 16.6: Submicron VLSI Memory Circuits", T. Mano, J. Yamada, J. Inoue, S. Nakajima, 1983 IEEE International Solid-State Circuits Conference
		ISSCC 84, Wednesday, February 22, 1984, Continental Ballrooms 6-9, 4:30pm, Session VIII A: 256K 1Mb DRAMs I, "WPM 8A.5: A Submicron VLSI Memory with a 4b-at-a-Time Built-in ECC Circuit", J. Yamada, T. Mano, J. Inoue, S. Nakajima, T. Matsuda, 1984 IEEE International Solid-State Circuits Conference

<b>Examiner Signature:</b> /Guy Lamarre/ (07/17/2006)	<b>Date Considered:</b>
<b>EXAMINER:</b> Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if in conformance and not considered. Include copy of this form with next communication to applicant.	

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### OTHER DOCUMENTS

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